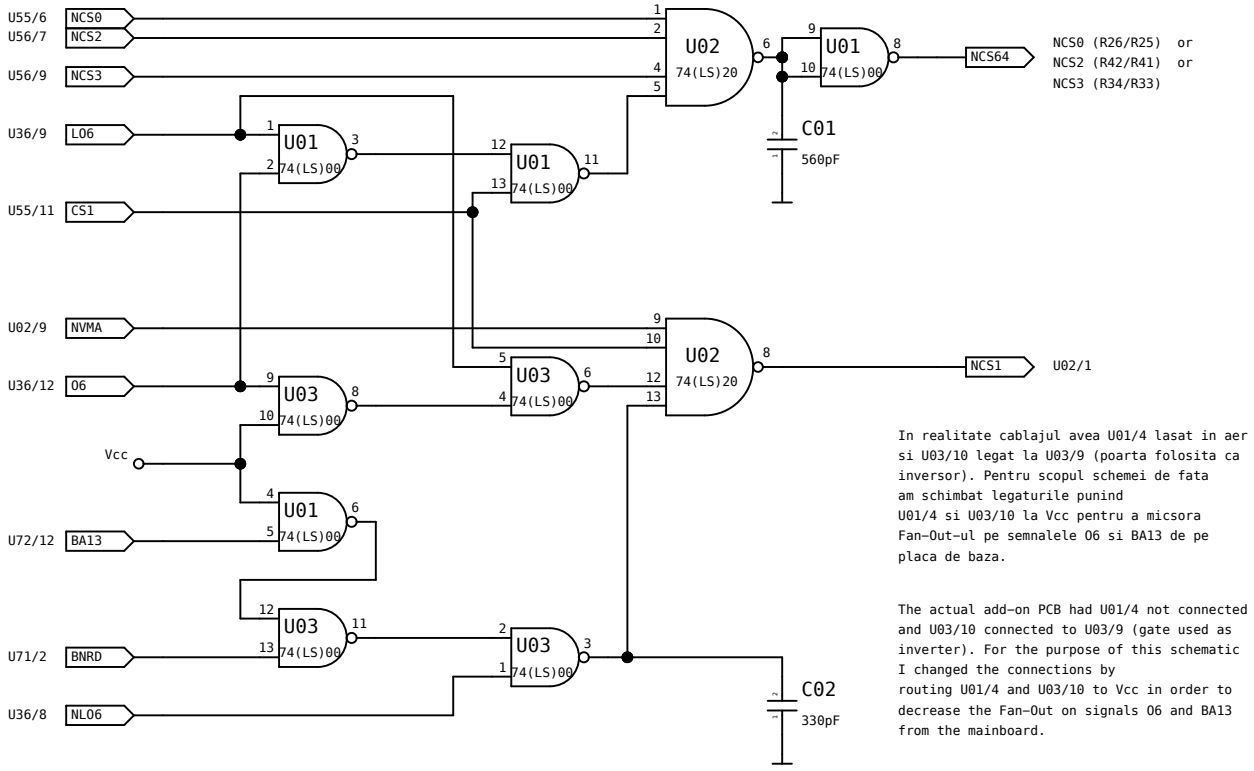
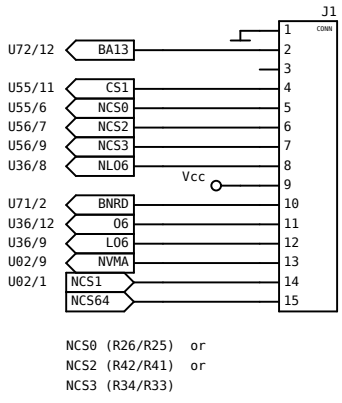


In realitate cablajul avea U01/4 lasat in aer si U03/10 legat la U03/9 (poarta folosita ca inversor). Pentru scopul schemei de fata am schimbat legaturile punind U01/4 si U03/10 la Vcc pentru a micsora Fan-Out-ul pe semnalele O6 si BA13 de pe placa de baza.

The actual add-on PCB had U01/4 not connected and U03/10 connected to U03/9 (gate used as inverter). For the purpose of this schematic I changed the connections by routing U01/4 and U03/10 to Vcc in order to decrease the Fan-Out on signals O6 and BA13 from the mainboard.



NCS0 (R26/R25) or
NCS2 (R42/R41) or
NCS3 (R34/R33)

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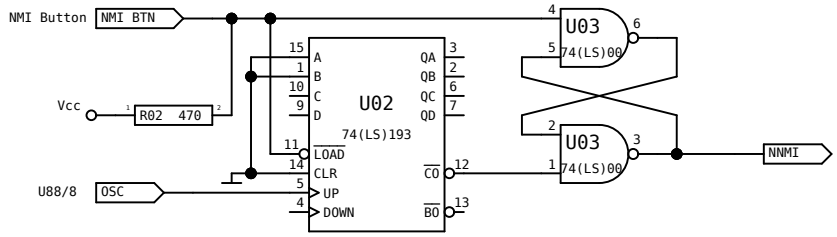
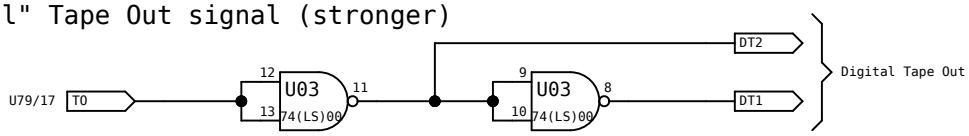


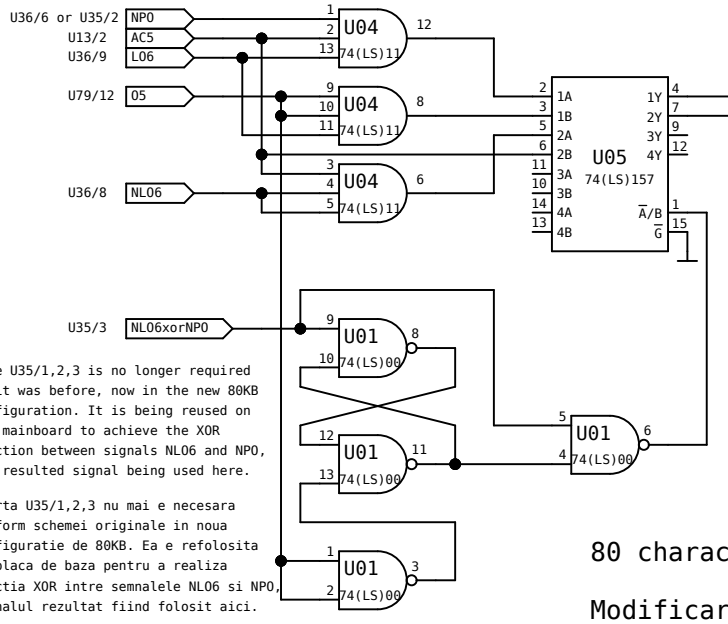
NMI Button Circuit

Circuit pentru buton NMI

"Digital" Tape Out signal (stronger)



Semnal digital de iesire pt. caseta (mai puternic)



Gate U35/1,2,3 is no longer required as it was before, now in the new 80KB configuration. It is being reused on the mainboard to achieve the XOR function between signals NLO6 and NPO, the resulted signal being used here.

Poarta U35/1,2,3 nu mai e necesara conform schemei originale in noua configuratie de 80KB. Ea e refolosita pe placa de baza pentru a realiza functia XOR intre semnalele NLO6 si NPO, semnalul rezultat fiind folosit aici.

On the mainboard side 1, there is a connection from U13/2 (AC5) to U14/2,9 and further to U15/2. For the purpose of the "80 char/line in CP/M modification" the connection must be cut right next to U15/2 (see cut #12 on mainboard side 1), preserving the connection between U13/2 and U14/2,9. Then signal "AC5new" will be routed to U15/2.

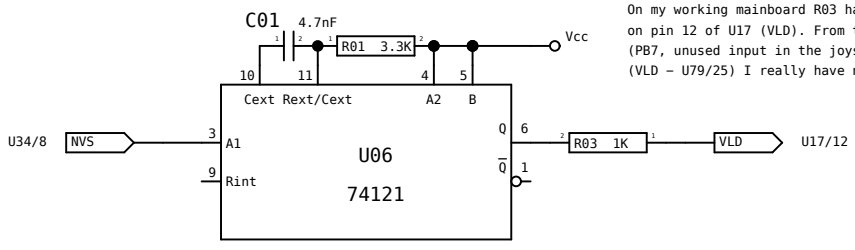
Pe placa de baza fata 1, exista un traseu de la U13/2 la U14/2,9 si apoi la U15/2. Pentru a realiza "modificarea de 80 caractere pe linie in CP/M" traseul trebuie taiat imediat linga U15/2, (vezi taietura #12 pe fata 1 a placii de baza), pastrind conexiunea dintre U13/2 si U14/2,9. Apoi semnalul "AC5new" va fi dus la U15/2,

80 characters per line in CP/M modification

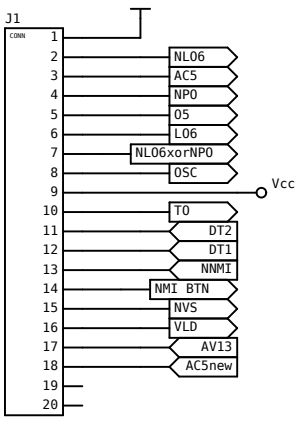
Modificarea de 80 caractere pe linie in CP/M

This circuit supposedly provides a signal (U06/6) to be applied to input U17/12 on the mainboard in order to generate the 20 ms interrupts to CPU (of course for that U17/12 should first be disconnected from VLD (U17/5) to which it is connected on the original mainboard). Due to not understanding this, back when I assembled the mainboard I left U17/12 connected to U17/5 (VLD) but in order to avoid shorting VLD to output U06/6 from this schematic I added R03. Of course, U06 is completely useless since this way U17/12 is still fed VLD.

Also, the 80K modification schematic aquired from others also contained a flip-flop (1/2 x 7474) used as divider by 2 on output U06/1, the resulting signal being called "SI/TRG0". In the original schematics, JEXA/9 (pin 9 of floppy interface connector) was connected to a signal "SI/TRG3" which actually did not exist anywhere. On my working mainboard, JEXA/9 is connected to NVS. This means the whole 74121 circuit is actually useless, just like the flip-flop above which I never used anyway.



On my working mainboard R03 had pin 1 soldered directly on the back of the board, on pin 12 of U17 (VLD). From there (U17/12) there was also a wire going to U79/25 (PB7, unused input in the joystick port), and the purpose of this connection (VLD - U79/25) I really have no idea what was (!!!)



Acest circuit se presupune ca ar furniza un semnal (la iesirea U06/6) care sa fie folosit la intrarea U17/12 pentru a genera intreruperile la fiecare 20 ms catre procesor (evident ca pentru asta intrarea U17/12 ar trebui mai intii deconectata de la semnalul VLD la care este legata pe placa de baza originala). Din cauza neintelegerii acestui fapt, la vremea cind am asamblat placa de baza am lasat U17/12 legat la U17/5 (VLD) dar pentru a nu scurtcircuita semnalul VLD cu semnalul dat de U06/6 din schema de fata am adaugat R03. Evident, U06 este absolut inutil de vreme ce in felul acesta U17/12 primeste practic tot semnalul VLD.

De asemenea, schema modificarii de 80K parvenita de la altii mai cuprindea si un bistabil (1/2 x 7474) folosit ca divizor cu 2 pentru iesirea U06/1, semnalul rezultat fiind denumit "SI/TRG0". In schemele originale, JEXA/9 (pin 9 conector interfata floppy de pe placa de baza) era legat la un semnal "SI/TRG3" care de fapt nu exista nicaieri. Pe placa mea de baza functionala, JEXA/9 este legat la NVS. Asta inseamna ca de fapt acest circuit cu 74121 este de fapt complet inutil, ca si bistabilul mentionat mai sus pe care oricum nu l-am folosit.

Pe placa mea de baza functionala R03 era lipita cu un pin direct pe dosul cablajului, pe pinul 12 al U17 (VLD). De acolo (U17/12) mai era facuta o legatura cu fir la U79/25 (PB7, o intrare nefolosita de la portul de joystick), iar scopul acestei legaturi (VLD - U79/25) nu pot sa-mi dau seama care ar putea fi (!!!)

TITLE Circuit suplimentar #2 Add-On Board #2	
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